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FORM PTO-1390
REV. 5-93

US DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEYS DOCKET NUMBER
P00.0665

U.S.APPLICATION NO. (if known, see 37 CFR 1.5)
09/530549

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE99/02778	**September 2, 1999**	**September 2, 1998**

TITLE OF INVENTION: **METHOD AND DEVICE FOR SYSTEM SIMULATION OF MICROCONTROLLERS/MICROPROCESSORS AND APPERTAINING PERIPHERAL MODULES**

APPLICANT(S) FOR DO/EO/US: **Albrecht Mayer**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay.
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of International Application (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2).

7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)) **(attached at back of English translation of application)**.

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98; **(PTO 1449, Prior Art, Search Report)**.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
    (SEE ATTACHED ENVELOPE)

13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information:
    a. ☒ Submission of Drawings
    b. ☒ Request for Approval of Drawing Changes
    c. ☒ EXPRESS MAIL #EL482397556US

U.S.APPLICATION NO (if known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/530549	PCT/DE99/02778	P00,0665

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5): Search Report has been prepared by the EPO or JPO ..... $840.00 International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) ... $760.00 No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO (37 C.F.R. 1.445(a)(2) ..... $450.00 Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2) paid to USPTO ..... $1,250.00 International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) ..... $ 98.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 840.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	6 - 20 =		X $ 18.00	$ 0.00	
Independent Claims	2 - 3 =		X $ 78.00	$ 0.00	
Multiple Dependent Claims			$270.00 +	$ 0.00	
			TOTAL OF ABOVE CALCULATIONS =	$ 840.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 C.F.R. 1.9, 1.27, 1.28)				$	
			SUBTOTAL =	$ 840.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
			TOTAL NATIONAL FEE =	$	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property +				**SEE ATTACHED ENVELOPE**	
			TOTAL FEES ENCLOSED =	$ 840.00	
			Amount to be refunded	$	
			charged	$	

a. ☒ A check in the amount of $ 840.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **08-2290**. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Hill & Simpson
A Professional Corporation
85th Floor Sears Tower
Chicago, Illinois 60606

SIGNATURE

Melvin A. Robinson
NAME

31,870
Registration Number

CERTIFICATE OF MAILING BY EXPRESS MAIL

"Express Mail" Mailing Label Number EL482397556US

Date of Deposit: May 2, 2000

I hereby certify that this correspondence is being deposited with the United States Postal "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10(c) on the date indicated above and is addressed to:

BOX PCT
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Case Number: P00,0665

International Application No.
PCT/DE99/02778

International Filing Date
September 2, 1999

Priority Date Claimed
September 2, 1998

Title: METHOD AND DEVICE FOR SYSTEM SIMULATION OF MICROCONTROLLERS/MICROPROCESSORS AND APPERTAINING PERIPHERAL MODULES

Applicants: Albrecht Mayer

Enclosed are the following documents:

PTO Form 1390 in duplicate
PCT Request Form
Translation of International Application into English
Information Disclosure Statement, PTO Form 1449 and references cited
Preliminary Amendment

Submission of Drawings (2 sheets - Figs.1-2)
Request for Approval of Drawing Changes

Fee: $840.00 filing fee

Postcard

Signature of person mailing document and fees

BOX PCT

IN THE UNITED STATES DESIGNATED/ELECTED OFFICE

OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER THE PATENT COOPERATION TREATY-CHAPTER II

AMENDMENT "A" PRIOR TO ACTION

APPLICANT(S):	Albrecht Mayer
ATTORNEY DOCKET NO.:	P00,0665
INTERNATIONAL APPLICATION NO.:	PCT/DE99/02778
INTERNATIONAL FILING DATE:	02 September 1999
INVENTION:	"METHOD AND DEVICE FOR SYSTEM SIMULATION OF MICROCONTROLLERS/MICROPROCESSORS AND APPERTAINING PERIPHERAL MODULES"

Assistant Commissioner for Patents

Washington, D.C. 20231

Sir:

Applicant herewith amends the above-referenced PCT application, and requests entry of the Amendment prior to examination in the United States National Examination Phase.

IN THE SPECIFICATION:

On page 1, cancel the title above line 4, and insert the following above line 4:

--TITLE

METHOD AND DEVICE FOR SYSTEM SIMULATION OF MICROCONTROLLERS/MICROPROCESSORS AND APPERTAINING PERIPHERAL MODULES

BACKGROUND OF THE INVENTION--;

in line 4, after "The" insert --present--, and preceding "simulation" insert -- a method for--.

On page 2, in line 5, cancel ", or respectively," substitute --or-- therefor;

in line 8, cancel "EP 0 777 180 A2" substitute --European Patent Application No. 0 777 180-- therefor;

in line 15, cancel "NB:" substitute --Note:-- therefor;

in line 24, cancel "[sic]".

On page 3, in line 3, insert a centered heading:

--**SUMMARY OF THE INVENTION**--;

in line 5, cancel "accelerated significantly" substitute --significantly accelerated-- therefor;

in line 7, after "achieved" insert --in accordance with the present invention--;

in line 20, cancel ", or respectively," substitute --or-- therefor;

in line 21, cancel "imulated/executed" substitute --simulated/executed-- therefor;

in line 22, cancel "partly in a simplified form [sic]" substitute --in a partly simplified form-- therefor.

On page 4, in line 1, cancel "one" substitute --an-- therefor;

in line 3, insert the following:

-- In an embodiment, there is provided a method for system simulation with simulated microcontrollers/microprocessors and appertaining peripheral modules, said method comprising the steps of:

in a first sequence of steps, simulating said microcontroller/microprocessor and said peripheral modules with predetermined signal patterns, said first sequence of steps having markers inserted therein;

in a second sequence of steps, interrogating and evaluating system states brought about by said simulation; and

interrupting said first sequence of steps for executing said second sequence of steps as dictated by said markers that have been

inserted into said first sequence, said second sequence of steps being executed in an accelerated operational mode that is adapted to said evaluation.--;

in line 4, after "achieved" insert --in accordance with the present invention--;

in line 9, insert the following:

-- In an embodiment, there is provided a system for carrying out a method for system simulation with simulated microcontrollers/microprocessors and appertaining peripheral modules, said method comprising the steps of:

in a first sequence of steps, simulating said microcontroller/microprocessor and said peripheral modules with predetermined signal patterns, said first sequence of steps having markers inserted therein;

in a second sequence of steps, interrogating and evaluating states of said system brought about by said simulation; and

interrupting said first sequence of steps for executing said second sequence of steps as dictated by said markers inserted into said first sequence, said second sequence of steps being executed in an accelerated operational mode that is adapted to said evaluation;

said system comprising:

a microprocessor control unit for simulating a module by generating signal patterns with an essentially precise clock cycle and for interrogating and evaluating states of said module that are brought about by said simulation during a program interrupt by activating an instruction set simulator.--;

in line 26, preceding "invention" insert --present--;

in line 28, cancel ", or respectively," substitute --or-- therefor.

On page 5, in line 4, insert the following:

-- These and other features of the invention(s) will become clearer with reference to the following detailed description of the presently preferred

embodiments and accompanied drawings.

DESCRIPTION OF THE DRAWINGS

Figure 1 is a block circuit diagram of an arrangement for overall system simulation according to the present invention.

Figure 2 shows an excerpt of steps of a CPU that are operated in accordance with the present inventive method.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS--;

cancel line 7;

in line 29, cancel ", or respectively," substitute --or-- therefor.

On page 6, cancel lines 8-15;

in line 18, preceding "invention" insert --present--;

in line 21, cancel "Pmn" substitute --PMn-- therefor;

in line 28, cancel "Pmn" substitute --PMn-- therefor.

On page 7, in line 14, cancel the comma;

in line 15, cancel "respectively,";

in line 21, preceding "inventive" insert --present--.

On page 8, in line 1, preceding "inventive" insert --present--;

in line 11, preceding "inventive" insert --present--;

below line 11, insert the following paragraph:

-- Although modifications and changes may be suggested by those of ordinary skill in the art, it is the intention of the inventors to embody within the patent warranted hereon all changes and modifications as reasonably and properly come within the scope of their contribution to the art.--.

IN THE CLAIMS:

On page 9, in line 1, cancel "Patent Claims" substitute --**I CLAIM AS MY INVENTION:**-- therefor.

Please cancel claims 1-6, substitute the following claims 7-12 therefor:

7. A method for system simulation with simulated microcontrollers/microprocessors and appertaining peripheral modules, said method comprising the steps of:

in a first sequence of steps, simulating said microcontroller/microprocessor and said peripheral modules with predetermined signal patterns, said first sequence of steps having markers inserted therein;

in a second sequence of steps, interrogating and evaluating states of said system brought about by said simulation; and

interrupting said first sequence of steps for executing said second sequence of steps as dictated by said markers inserted into said first sequence, said second sequence of steps being executed in an accelerated operational mode that is adapted to said evaluation.

8. The method as claimed in claim 7, wherein said first sequence of steps provides a clock-cycle-based simulation of said microcontroller/microprocessor and of said peripheral modules.

9. The method as claimed in claim 7, wherein said first sequence of steps is a series of consecutive program codes.

10. The method as claimed in claim 9, wherein said markers are formed by one of opcodes or opcode sequences that are not usually used in said program code.

11. The method as claimed in claim 7, wherein peripheral modules that were specified during said second sequence of steps are functionally cosimulated.

12. A system for carrying out a method for system simulation with simulated microcontrollers/microprocessors and appertaining peripheral modules, said method comprising the steps of:

in a first sequence of steps, simulating said microcontroller/microprocessor and said peripheral modules with predetermined signal patterns, said first sequence of steps having markers inserted therein;

in a second sequence of steps, interrogating and evaluating states of said system brought about by said simulation; and

interrupting said first sequence of steps for executing said second sequence of steps as dictated by said markers inserted into said first sequence, said second sequence of steps being executed in an accelerated operational mode that is adapted to said evaluation;

said system comprising:

a microprocessor control unit for simulating a module by generating signal patterns with an essentially precise clock cycle and for interrogating and evaluating states of said module that are brought about by said simulation during a program interrupt by activating an instruction set simulator.

IN THE ABSTRACT:

On page 11, cancel lines 1-3, insert the following centered heading at line 1:

--**ABSTRACT OF THE DISCLOSURE**--;

in line 6, cancel "is described";

in line 7, after "simulating" cancel "the" substitute --a-- therefor, and after "and" cancel "the";

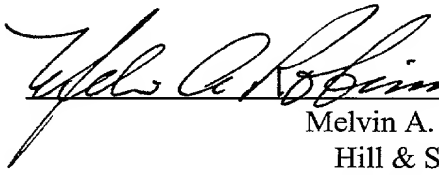
cancel line 15.

REMARKS:

The present Amendment revises the specification, drawings and claims to conform to United States patent practice, before examination of the present PCT application in the United States National Examination Phase. All of the changes are editorial and no new matter is added thereby. Claims 1-6 have been canceled. New claims 7-12 are patentably distinguishable from the known prior art.

Early examination on the merits is respectfully requested.

Respectfully submitted,



~~(Reg.~~ No. 31,870)

Melvin A. Robinson
Hill & Simpson
A Professional Corporation
85th Floor - Sears Tower
Chicago, Illinois 60606
(312) 876-0200 ext. 3899
Attorneys for Applicant(s)

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IN THE UNITED STATES DESIGNATED/ELECTED OFFICE

OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER THE PATENT COOPERATION TREATY-CHAPTER II

REQUEST FOR APPROVAL OF DRAWING CHANGES

APPLICANT(S):	Albrecht Mayer
ATTORNEY DOCKET NO.:	P00,0665
INTERNATIONAL APPLICATION NO.:	PCT/DE99/02778
INTERNATIONAL FILING DATE:	02 September 1999
INVENTION:	"METHOD AND DEVICE FOR SYSTEM SIMULATION OF MICROCONTROLLERS/MICROPROCESSORS AND APPERTAINING PERIPHERAL MODULES"

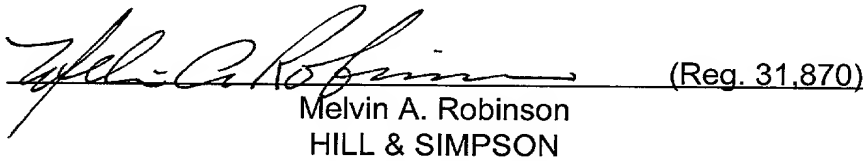
Assistant Commissioner for Patents

Washington, D.C. 20231

S I R:

Applicant herewith requests approval of the drawing changes in FIGs. 1 and 2 as shown on the drawing copies marked in red attached hereto.

Submitted by,



(Reg. 31,870)

Melvin A. Robinson
HILL & SIMPSON
A Professional Corporation
85th Floor - Sears Tower
Chicago, Illinois 60606
Telephone: 312/876-0200 - Ext. 3899
Attorneys for Applicant(s)

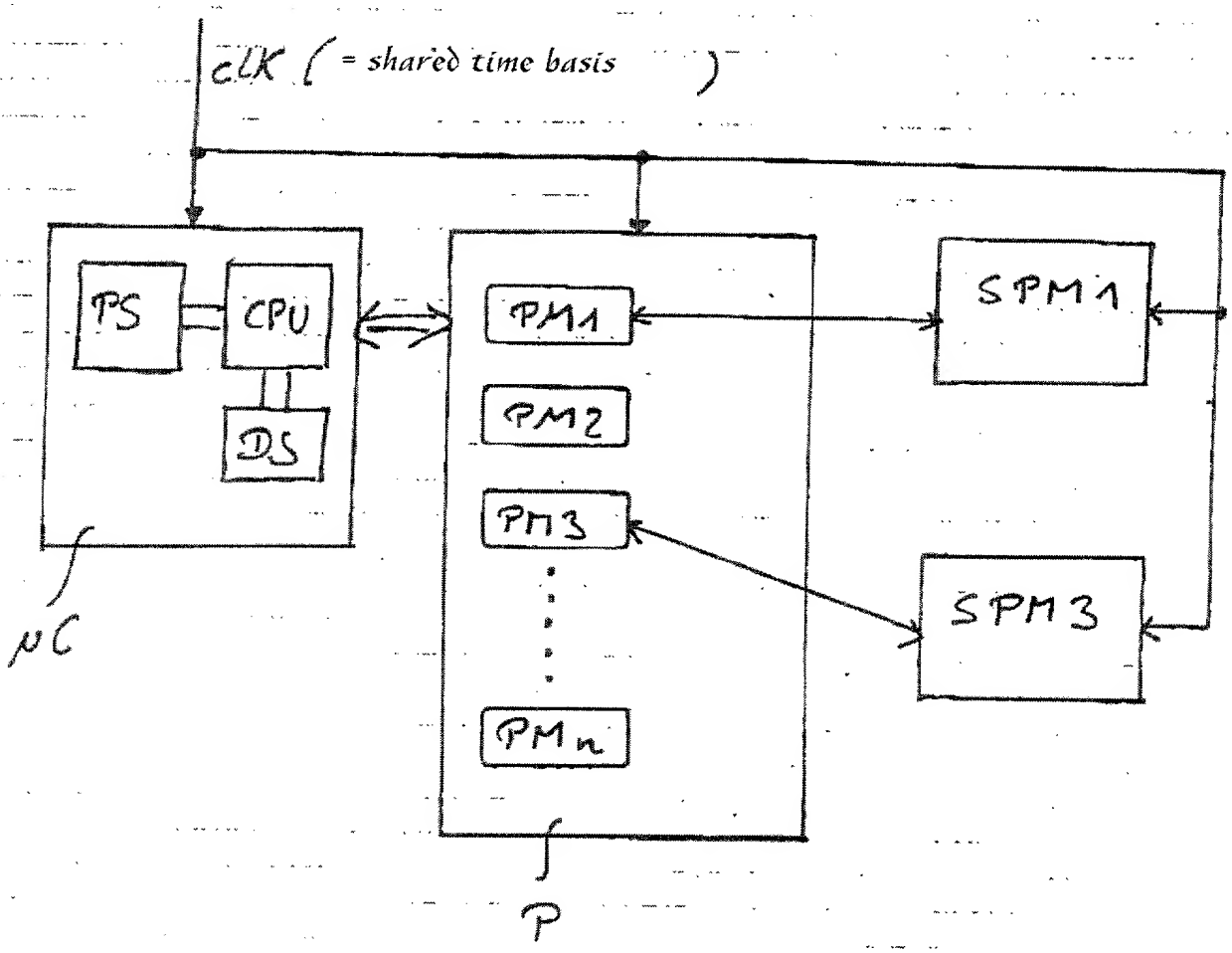


Fig. 1

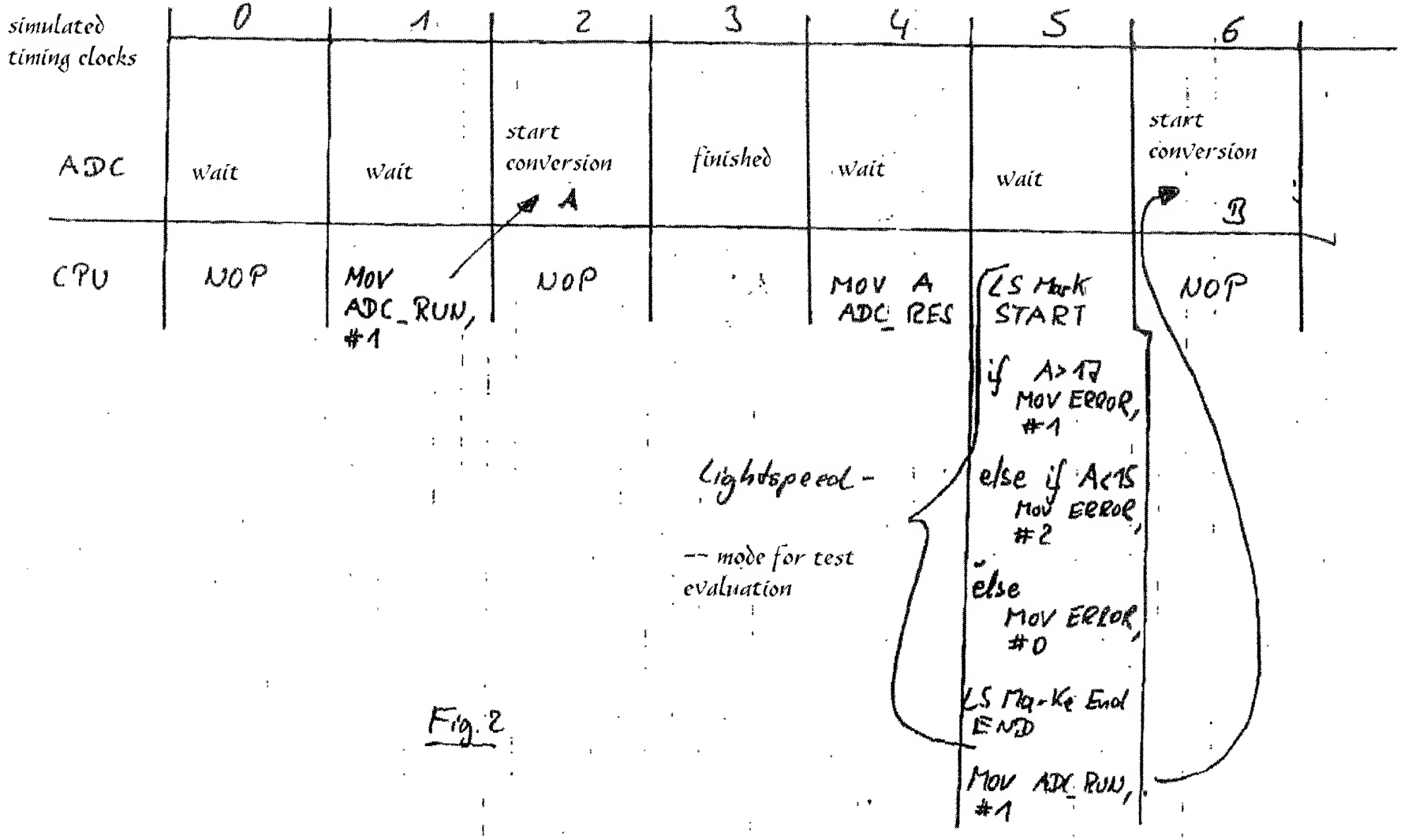


Fig. 2

Method and Device for System Simulation of Microcontrollers/Microprocessors and Appertaining Peripheral Modules

The invention relates to simulation and to a device for carrying out the method.

Simulations of computer modules serve the optimizing of the system architecture of a computer, the development of suitable software, and the early detection of errors before the hardware is actually realized. In this way significant savings can be gained in the development process.

The pattern of a system should be understood as the arrangement of a microcontroller with peripheral modules and an external environment. The microcontroller specifically is the pure central processing unit (CPU). But microcontroller chips generally also have peripheral modules on the chip as well. Peripheral modules can have a wide variety of tasks; for instance, analog to digital converters (ADC), counters, serial interfaces, and so on. In this regard, peripheral modules are always hardware modules.

If, for example, a peripheral module is being developed for a microcontroller, this module is simulated with typical signal patterns, and is configured and controlled by the preferably also simulated microprocessor. The simulated states of the module are interrogated and evaluated by the microprocessor. Since the simulations have a precise clock cycle, all modules are always cosimulated when the microcontroller evaluates the states of the peripheral module. This evaluation can prolong the simulation time considerably.

However, particularly in the case when several modules are simulated at the same time, the total run can require a relatively long period of time, especially since the

simulation of all modules always continues, even when the states of one module are being evaluated, owing to the unified processor clock.

Hitherto, the prolonged simulation time was accepted into the bargain, or the evaluation of the peripheral states was reduced to a minimum, or respectively, was not done during the system simulation.

EP 0 777 180 A2 already teaches a method for simulating and emulating systems, consisting of software and (simulated) hardware components. The method provides the possibility of interaction between the hardware and software components while at the same time the two systems are largely decoupled.

The basic idea of this method is to let the clocks of the components run independently and to synchronize them only at those points at which an interaction between the systems occurs, and only for the strictly necessary number of cycles. (NB: the term "clock of a component" is used in the sense of the clock that measures the simulated time). The real time is of course equal for all component simulations. To clarify the difference: One second of simulated time can last an hour in real time, for example.

The advantage of this method is that a rapidly simulatable system component is not slowed down by a slow one. This is of course also true when the interaction between the components is small. On the other hand, when the two clocks are rigidly synchronized, then the speed of simulation can never be higher than that of the slowest comonents. **[sic]**

The disadvantage of the method is that it cannot be tolerated in many system simulations that the clocks of the components do not have absolute synchronization. In addition to this, simulation runs cannot be fully reproduced, since the relative

position of the clocks of the subcomponents are influenced, for instance by the loading of the simulation computer.

It is thus the object of the invention to set forth a method and a device of the above mentioned type with which the overall simulation run can be accelerated significantly.

For the method, this object is inventively achieved in that a first sequence of steps is provided for simulating the module with predetermined signal patterns, and a second sequence of steps is provided for interrogating and evaluating system states that are induced by the simulation, whereby the first sequence is interrupted for the purpose of executing the second sequence as dictated by markers that have been inserted into the first sequence, and the second sequence is executed in an accelerated operational mode that has been adapted to the evaluation.

During the normal simulation, the microcontroller and the peripheral module are simulated with a precise clock cycle, whereas in the accelerated code execution "simulated" time does not elapse; that is, the program part is processed in a kind of instruction set simulator.

The accelerated operational mode, or respectively, code execution, should be understood as meaning that only a small part of the system is imulated/executed, and even that partly in a simplified form **[sic]**. An example is that only the CPU processes program code as instruction set simulator, and the rest of the system is not simulated. An example of a peripheral module is a serial interface, which files data in the output buffer directly in the memory for the simulation evaluation. In the case of the non-accelerated operational mode, over several clock cycles the serial interface would convert the data bit by bit into an output signal, which would then be received bit by bit by a receiver, assembled, and filed in the memory.

In one embodiment it is provided that certain peripheral modules are also cosimulated purely functionally during the accelerated code execution.

For the system for carrying out the method, the object is achieved in that a microprocessor control unit is provided for simulating the module by generating clock-cycle-based signal patterns and for interrogating and evaluating the system states brought about by the simulation during a program interruption by activating an instruction set simulator.

A particular advantage of these solutions is that an appreciable reduction of the time required for the overall run can be achieved by separating the actual system simulation from the evaluation of the simulation results, since in the evaluation phase the processor is not loaded with the then superfluous simulation processes, and on the other hand the evaluation itself runs faster due to the accelerated operational mode.

Further advantages consist in the ability of the program to monitor and test the states of the peripheral module comprehensively. It is not necessary to keep an additional external evaluation program current. Beyond this, the evaluation can be completely prevented from influencing the time characteristic of the program.

Beyond this, a critical advantage consists in the ability to use the program that was designed for the system simulation and for the simulated microcontroller for the actually realized microcontroller – that is to say, the one cast in silicon – following the removal of the provided markers.

In summary, the invention for simulating computer modules essentially consists in the dividing of the system simulation into two subsimulations from the standpoint of the microcontroller, or respectively, the microprocessor: on one hand, the actual system simulation; that is, the simulation of the peripheral module, which is simulated with

typical signal patterns; and on the other hand, the simulation of the microcontroller. The second subsimulation relates to the evaluation of interrogated system states. When the evaluation phase is accelerated by the proposed method, not only does the simulated time characteristic become more precise, but the total simulation time is also reduced significantly.

The inventive method is detailed below with the aid of an exemplifying embodiment.

The simulation of a type 8051 microcontroller is taken as exemplifying embodiment.

In the simulation model of the 8051 microcontroller it is assumed that the inventive method has been implemented. For example, the assembler code for the simulation model of the 8051 microcontroller can read as follows:

```
...(program code)...
db 0a5h, "1+"      ; **** start lightspeed mode

mov sbuf, #"H"     ; visible in the console window
mov sbuf, #"i"
mov sbuf, #"!"
db 0a5h, "1-"      ; **** end lightspeed mode
mov sbuf, #"H"     ; visible on the internal bus, but not in the console window
...(program code)
```

The program code is directly processed between the markers without the simulation model requiring clock pulse edges. The thus processed program code is located before the markers and after the markers and is indicated above solely by dots (...). The opcode a5h, which is not ordinarily used, with the subsequent ASCII characters "1+" and "1-" for starting, or respectively, stopping the second sequence of steps can

be used as markers. Suitable opcode sequences can also be used. The second sequence of steps is referred to below as "lightspeed".

During this second sequence of steps, the serial interface of the simulation model of the 8051 microcontroller is simulated in that all outputs by the simulation model on its register SBUF are written directly onto the console window.

The invention is detailed below with the aid of another exemplifying embodiment in connection with the Figures. Shown are:

Figure 1: a block circuit diagram of an arrangement for overall system simulation according to the invention, and

Figure 2: an excerpt of steps of a CPU that are operated in accordance with the inventive method.

Figure 1 shows a block circuit diagram for an arrangement for overall system simulation according to the invention. The block circuit diagram shows the core of a microprocessor μC, which contains a CPU unit, a program memory PS, and a data storage unit DS; the microprocessor μC stands in connection with a peripheral unit P comprising several peripheral modules PM1, PM2, PM3 to Pmn. In addition, two blocks are represented for the simulated environment of the peripheral module PM1 and of the peripheral module PM3. The blocks are referenced SPM1 and SPM3. The block SPM1 could be a simulated sine generator, for example. The block referenced SPM3 could be a simulated console. An analog/digital converter can be provided as peripheral module PM1; a counter, as peripheral module PM2; and a serial interface, as peripheral module PM3. All components – that is, the microprocessor μC, the peripheral modules PM1 to Pmn, and the simulated environments for the peripheral

modules – stand in connection to each other with a common time base c1k, that is to say, with a common clock.

In an arrangement such as this, a system simulation could look as follows: The peripheral module PM1 – i.e. an analog/digital converter, for example – measures the voltage of the simulated sine generator and triggers an interrupt after each measurement. The CPU then reads the value from the result register of the analog/digital converter and writes it into the data storage unit DS. After a certain number of measurements, the CPU switches into the accelerated mode and evaluates the measurements. After completing this, it switches back into the normal module, and the simulation continues at precisely the point at which the changeover occurred. The system simulation is therefore completely unaffected by the evaluation.

Figure 2 shows the status of the analog/digital converter (ADC) and the CPU, or respectively, their instructions, charted over simulated time cycles 0 to 6. The CPU accordingly starts an ADC conversion and copies the result into memory. In the lightspeed mode, for the purpose of the test evaluation it is tested whether the expected value 16 ± 1 was measured. This test is without influence on the overall system simulation, since the conversion 2 is started without delay.

In the inventive method, the "clocks of all subcomponents" are basically rigidly coupled and run synchronously. The sole exception is what is known as lightspeed mode, in which the clock of the hardware components is quiescent though the software still runs on the CPU. Before the software accesses the hardware, the lightspeed mode must be explicitly exited, which is triggered by special markers that are otherwise not present in the program.

The basis for the two different modes in the inventive method is the ability to monitor the clock of all subcomponents completely. This can be advantageously utilized for two applications:

1. On the simulated CPU, test programs can be executed without simulated time expiring and thus without influencing the system simulation itself.

2. The simulation can be accelerated when the software runs only on the CPU without the clock of the hardware components continuing to run.

Unlike the known methods, the inventive method is deterministic and reproducible.

Patent Claims

1. Method for system simulation with simulated microcontrollers/microprocessors and appertaining peripheral modules,
characterized by
a first sequence of steps for simulating the microcontroller/microprocessor and the peripheral modules with predetermined signal patterns, and
a second sequence of steps for interrogating and evaluating system states brought about by the simulation;
whereby the first sequence is interrupted for the purpose of executing the second sequence as dictated by markers that have been inserted into the first sequence, and the second sequence is executed in an accelerated operational mode that is adapted to the evaluation.

2. Method as claimed in claim 1,
characterized in that
the first sequence of steps provides a clock-cycle-based simulation of the microcontroller/microprocessor and of the peripheral modules.

3. Method as claimed in claim 1 or 2,
characterized in that
the first sequence of steps is a series of consecutive program codes.

4. Method as claimed in claim 3,
characterized in that
the markers are formed by opcodes or opcode sequences that are not usually used in the program code.

5. Method as claimed in one of the claims 1 to 4,

characterized in that

peripheral modules that were specified during the second sequence of steps are functionally cosimulated.

6. System for carrying out the method as claimed in one of the claims 1 to 5, characterized by

a microprocessor control unit for simulating the module by generating signal patterns with an essentially precise clock cycle and for interrogating and evaluating the module states that are brought about by the simulation during a program interrupt by activating an instruction set simulator.

Abstract

Method and Device for System Simulation of Microcontrollers/Microprocessors and Appertaining Peripheral Modules

A method for system simulation is described, which is distinguished by a first sequence of steps for simulating the microcontroller/microprocessor and the peripheral modules using predetermined signal patterns and by a second sequence of steps for interrogating and evaluating system states that are brought about by the simulation. In order to carry out the second sequence, the first sequence is interrupted as dictated by markers that have been inserted into the first sequence, and the second sequence is executed in an accelerated operational mode that has been adapted to the evaluation.

Figure 1

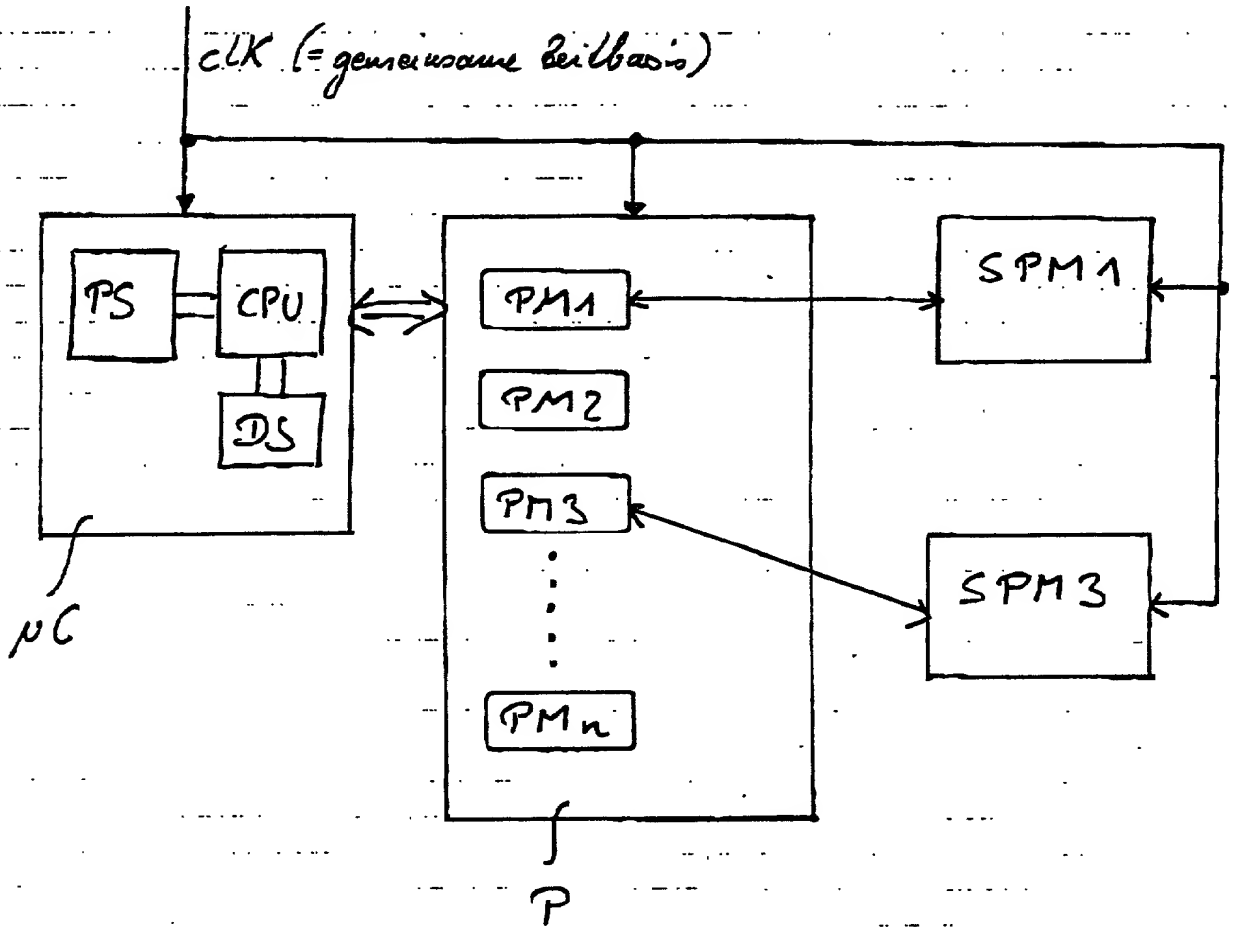

clk (= gemeinsame Zeitbasis)
PS
CPU
DS
µC
PM1
PM2
PM3
PMn
P
SPM1
SPM3

Fig. 1

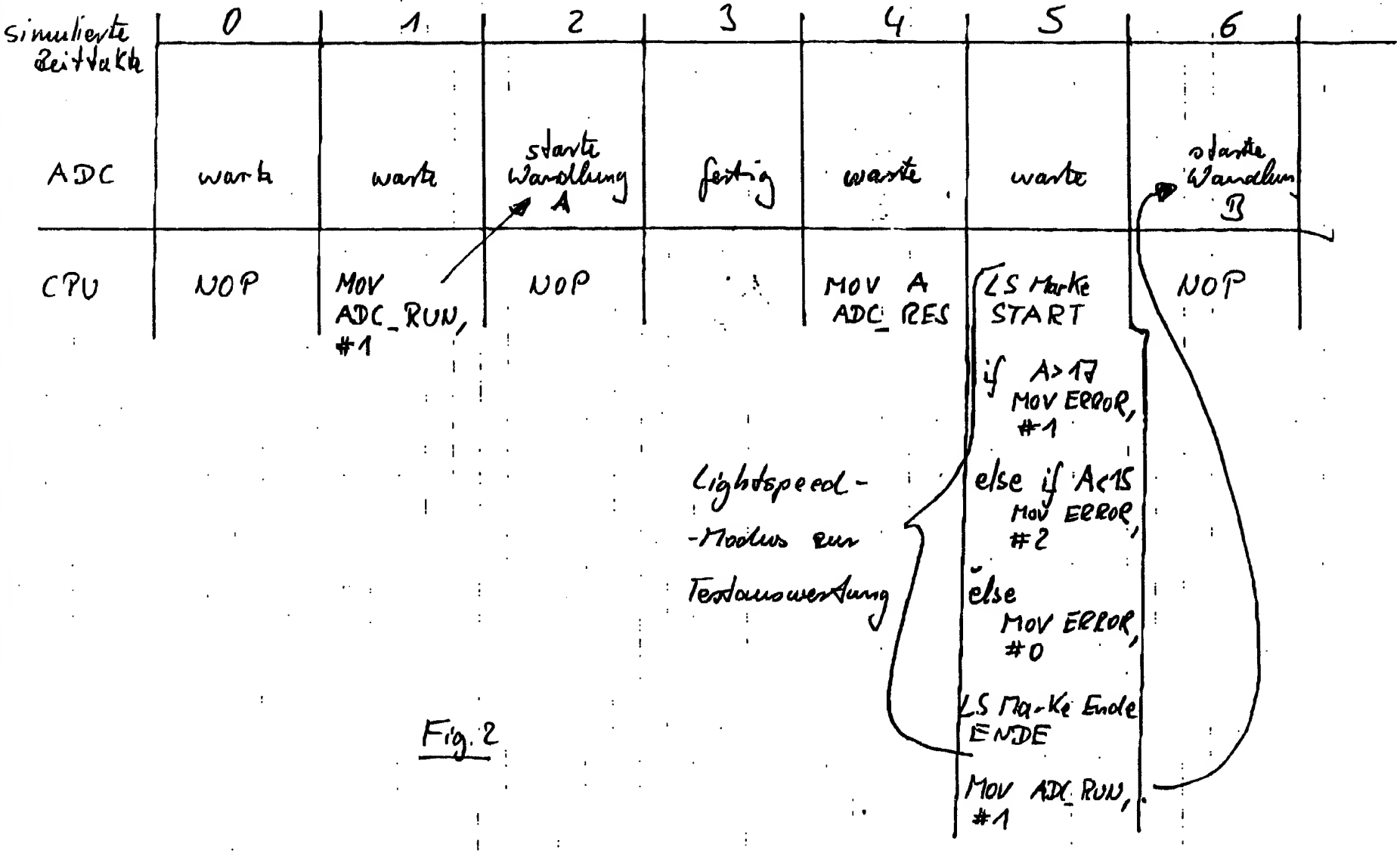


Fig. 2

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
ERKLÄRUNG FÜR PATENTANMELDUNGEN MIT VOLLMACHT
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für des dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND DEVICE FOR SYSTEM SIMULATION OF MICROCONTROLLERS/MICROPROCESSORS AND APPERTAINING PERIPHERAL MODULES

deren Beschreibung

(zutreffendes ankreuzen)

☐ hier beigefügt ist.

☐ am _____ als
PCT internationale Anmeldung
PCT Anmeldungsnummer _____
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

the specification of which

(check one)

☐ is attached hereto

☒ was filed on September 2, 1999, as
PCT international application
PCT Application No. PCT/DE99/02778
and was amended on _____
(if applicable)

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign applications
Priorität beansprucht

			Priority Claimed	
DE 198 40 033.0	Germany	September 2, 1998	☒	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein
			☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein
			☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein

Ich beanspruche hiermit germäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35, United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122 I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Eklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

10

And I hereby appoint Messrs. John D. Simpson (Registration No. 19,842), Dennis A. Gross (24,410), Robert M. Barrett, (30,142), Steven H. Noll (28,982), Kevin W. Guynn (29,927), Robert M. Ward (26,517), Brett A. Valiquet (27,841), Edward A. Lehman (22,312), David R. Metzger (32,919), James D. Hobart (24,149), Melvin A. Robinson (31,870), Joseph P. Reagen (35,332), Michael R. Hull (35,902), Michael S. Leonard (37,557), William E. Vaughan (39,056) and Lewis T. Steadman (17,074), all members of the firm of Hill & Simpson, A Professional Corporation

Telefongespräche bitte richten an:
(Name und Telefonnummer)

Direct Telephone Calls to: (*name and telephone number*)

312/876-0200
Ext. 3261

Postanschrift:

Send Correspondence to:

~~HILL & SIMPSON~~
A Professional Corporation
85th Floor Sears Tower, Chicago, Illinois 60606

Voller Name des einzigen oder ursprünglichen Erfinders: ALBRECHT MAYER	*Full name of sole or first inventor:*
Unterschrift des Erfinders x A. Mayer Datum 2000-05-05	Inventor's signature Date
Wohnsitz Deisenhofen, Germany DEX	Residence
Staatsangehörigkeit German	Citizenship
Postanschrift Jägerstr. 16	Post Office Address
D-82041 Deisenhofen Bundesrepublik Deutschland	

(Bitte entsprechende Informationen und Unterschriften im Falle von weiteren Miterfindern angeben).

(Supply similar information and signature for subsequent joint inventors).